

# Comparative Analysis of Memristor based Synaptic Circuits for Neuromorphic Architectures



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**Abstract**

Memristor is one of the fundamental electrical elements, which has recently been successfully built. Memristor is being used extensively as synapses in neuromorphic applications. A common method for developing memristor based synaptic circuits is to store synaptic weight values within memristors as resistance values. It requires use of the continuous resistance (memristance) range available in the memristors to store the weights. In this paper, we study how different compact synaptic circuits implemented using  $TiO_2$  memristors to perform zero, negative, and positive synaptic weightings. Results of different memristor based circuits, based on pulsed input signals, are compared, analyzed and presented using  $TiO_2$  memristors via simulations.

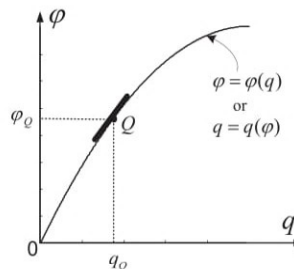
**Key words** – Memristor, Memristance, synapses, neuromorphic.

**I. Introduction**

The existence of the “memristor” as the fourth basic circuit element was predicted by Leon Chua in 1971 [1]. The prediction was based on symmetry and a missing relationship between an independent pair of the four fundamental circuit variables: current ( $i$ ), voltage ( $v$ ), charge ( $q$ ), and flux linkage ( $\phi$ ). The three basic circuit elements, resistor, inductor and capacitor are defined by a relationship between  $v$  and  $i$ ,  $\phi$  and  $i$ , and  $q$  and  $v$ , respectively, but the relationship between  $q$  and  $\phi$  was missing. For the sake of symmetry and completeness, the memristor was postulated in [1] as the fourth basic two-terminal circuit element characterized by a relationship between  $q$  and  $\phi$ .

Memristor is defined in [2] by a state-dependent Ohm’s law between the memristor-voltage  $v$  and memristor-current  $i$  as,

$$v = M(x_1, x_2, \dots, x_n) i \tag{1}$$



**Fig. 1 Nonlinear function between flux and charge. The memristance  $M(q)$  can be obtained by calculating the slope at  $q = q_e$**

where  $M$  is called the memristance and  $x_i'$  are the state variables. The state variables  $x_1, x_2, \dots, x_n$  are defined by “ $n$ ” differential equations called the associated state equations, as follow:

$$dx_k/dt = f_k(x_1, x_2, \dots, x_n; i), \quad k = 1, 2, \dots, n \quad (2)$$

In the special case where the device possesses only a single state variable  $x$  and  $f(x, i) = i$ , then  $x = q$  is the charge entering the memristor and the device is called an “ideal memristor”. The memristor is defined by,

$$v = \frac{d\phi(q)}{dq} \frac{dq}{dt} = M(q)i \quad (3)$$

where  $\phi$  and  $q$  denote the flux and charge, respectively. Thus, the memristance  $M(q)$  can be interpreted as the slope at the operating point  $q = q_0$  on the memristor  $\phi - q$  curve as in Fig. 1. If the  $\phi - q$  curve is nonlinear, the resistance will vary with the operating point. Since the resistance in this type of device is variable depending upon the operating point  $q = q_0$ , and since  $q = q_0$  remains fixed when  $v(t) = 0$  and  $i(t) = 0$ , the device can be used as a non-volatile memory. A dynamical system described in [2] by equations

$$v = M(x)i \quad (4)$$

$$M(x) = R_{ON}x + R_{OFF}(1-x) \quad (5)$$

$$dx/dt = Ki \quad (6)$$

is an example of a memristor, where  $i$  is the input current,  $v$  is the output voltage,  $R_{ON}, R_{OFF}$  and  $K$  are the system parameters,  $x$  is the state variable, and  $M(x)$  is its memristance.

The researchers from *hp* group has announced the successful development of a very compact memory element made of Titanium Dioxide [2], which exhibited the pinched hysteresis loop fingerprint of memristors.

In neural networks, incoming signal are multiplied with synaptic weights and outputs are obtained by passing through activation functions after the summation of the weighted input signals. Hardware implementation of the neural networks might be an essential step to solve the real time processing problem of neural networks. The success of each neural network hardware design depends largely on the trade-offs between accuracy, chip area and processing speed.

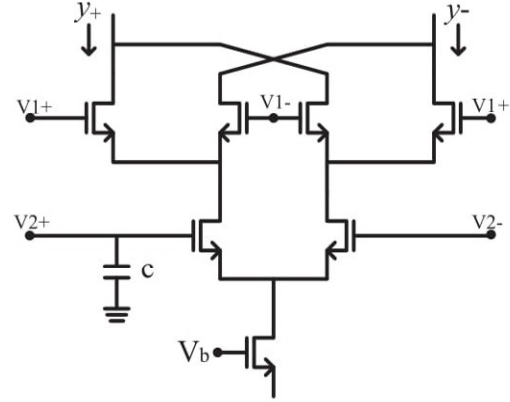


Fig. 2 Conventional CMOS synaptic circuit [3].

Unlike their digital counterparts, analog implementations are usually more efficient in terms of chip area and processing speed but they have limited accuracy which arises due to spatial non-uniformity of the analog components and their non-ideal responses. In addition, another major bottleneck in ANN hardware is the implementation of nonvolatile weight storage [4]. Resistors are static and cannot be changed once fabricated, thus they can be used only for non-learning hardware. Capacitors have short synaptic weights retention time due to charge leakage and require dynamic weight updating at frequent intervals. Floating gate transistors have been used successfully as synapses in conjunction with analog multipliers, but they suffer from high non-linearity in synaptic weightings. Memristor is a two terminal electrical element, which exhibits features of biological synapse under the excitation of input voltage or current pulses: its resistance can be altered in a manner, similar to bio-neurons, to emulate change in synaptic weight. Likewise the two memristors with anti serial connection can be used to generate both positive and negative weights. Composite behaviour of memristor circuits has been published in [5] which led to explore the varieties of applications of memristors. Recently few artificial synapses consisting of multiple identical memristors in a bridge-like fashion capable of performing signed synaptic weights were proposed in [6-7]. Memristor bridge circuit which is composed of four identical memristors is able to perform zero, negative and positive synaptic weightings is developed. Together with three additional transistors, the memristor bridge weighting circuit is able to perform synaptic operation for neural cells. By programming different values on each memristor of the memristor bridge circuit,



arbitrary weighting values can be set on the memristor bridge synapses.

The unique features of memristor-based neural architectures are their pulse-based operation, compact and adjustable weighting, non-volatile memory and linearly synaptic operation. In this paper, several memristor based synaptic circuits are studied and analyzed.

## II. Conventional CMOS synapse

Normally, CMOS analog multipliers are employed to compute the multiplication between input signals and weights in neural networks [2]. As the neural networks have massive interconnectivity and are parallel in nature, it is required that the multipliers should be smaller, consume low power and non-volatile. The multiplication between weights and input signals should be linear. However, it is very difficult to get the

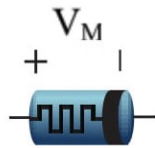


Fig. 3 A single memristor

Above features in CMOS analog multipliers. To implement such an immense amount of processing into a chip, extremely high density of analog multiplier is needed. Multiplication in a typical analog Gilbert circuit is usually implemented with at least seven transistors, as shown in Fig. 2, operating in a nonlinear and hence power-hungry regime. Therefore, significant nonlinearity is unavoidable in multiplication processing with conventional CMOS transistor circuits.

## III. Memristor Synapses

### A. Single Memristor Synapse

The memristance/memductance of a two-terminal memristor as shown in Fig. 3 can be varied by varying the current passing through it such that a memristor can be used as a synapse. The memductance of the memristor is analogous to the strength of the synapse. As memristor is a non-volatile device it retains its conductance when there is no external input, and the conductance can be changed by applying appropriate external signal to emulate change in synaptic weight.

### B. Two Memristor Synapse

Though a single memristor can be efficiently implemented as synapse in neural learning circuits, a single memristor lacks the ability to emulate negative weights which are commonly encountered when implementing artificial neural learning rules like back-propagation. But negative weights can be realized by utilizing other measurable quantities like current or voltage across appropriately connected memristor(s).

It consists of two identical anti-serial memristors with the polarities indicated as in Fig. 4. When an input pulse  $V_{in}$  is applied to the circuit, the memristance of each memristor increases or decreases depending on the polarity. For instance, if positive  $V_{in}$  is applied, the memristance of M1 decreases whereas the memristance of the reversely biased memristor M2 increases. Similarly, if negative  $V_{in}$  is applied the memristance of M1 increases whereas that of M2 decreases. The difference in the voltage drop across the memristor M1 and M2 then can be utilized to achieve positive and negative synaptic weights.

If  $V_{in}$  is applied to the circuit shown in Fig. 4, then using KVL, the input voltage is the sum of the voltage drop across memristor M1 and the voltage drop across memristor M2. The individual voltage drops across M1 and M2 are given as,

$$v_{M1} = \left( \frac{M1}{M1 + M2} \right) v_{in} \quad (7)$$

$$v_{M2} = \left( \frac{M2}{M1 + M2} \right) v_{in} \quad (8)$$

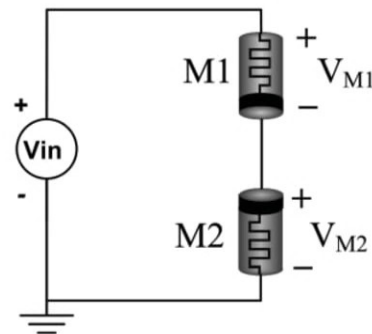


Fig. 4 Two anti-serially connected memristors

Then, the voltage of interest is the voltage difference between  $v_{M2}$  and  $v_{M1}$  given as

$$v_{out} = v_{M2} - v_{M1} = \left( \frac{M2 - M1}{M1 + M2} \right) v_{in} \quad (9)$$

From Eq. (9) we see that the arrangement in Fig. 4 performs synaptic weighting of the input signal  $V_{in}$ , where the output is a weighted function of the input and the weighting function is given as

$$\alpha = \left( \frac{M2 - M1}{M1 + M2} \right) \quad (10)$$

The conditions for the anti-serial memristor arrangement to function as weight in different regimes is listed as follow.

- If  $M2 > M1$ , positive synaptic weight
- If  $M2 < M1$ , Negative synaptic weight
- If  $M2 = M1$ , Zero synaptic weight

### C. Five-Memristors Bridge-Based Synapses

In the memristor weighting circuit, both positive and negative multiplications are performed via a charge-dependent Ohm's law ( $v = M(q) \times i$ ). The circuit is composed of five memristors with bridge-like connections together with one differential amplifier. It operates like an artificial synapse with pulse-based processing and non-volatile adjustable weightings.

The sign-setting, weight-setting (positive or negative) and the processing signals are applied through a common input terminal. It is assumed that the voltage which is generated internally by current signal makes the same amount of memristance change as that by the same magnitude of the externally applied voltage. The memristor  $M_w$  at the center plays the weighting role of the synapse and the other memristors,  $M_{s1}$ ,  $M_{s2}$ ,  $M_{s3}$  and  $M_{s4}$  function as switches for selecting the weighting sign.

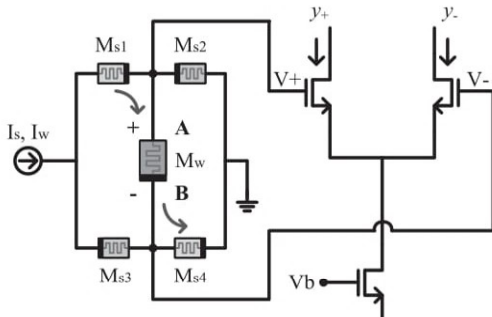


Fig. 5 Memristor-based synaptic circuit.

The memristors alter the sign of the input voltage of the differential amplifier by switching the on-off states of the memristors in the manner of a bridge circuit. Though five memristors are employed to emulate a synapse in circuit, the total area of the five memristors is less than that of a single transistor.

### Sign Setting

Prior to weight setting or multiplication processing, the sign of the synaptic weight is set first. This is implemented by applying a strong current pulse (high amplitude or wide current pulse) to change the memristances toward one of the two extreme values (In the  $TiO_2$  memristor it is assumed that a turn-on resistance  $116 \Omega$ , and turn-off resistance  $15.98 K\Omega$ ).

When a positive wide pulse is applied at the input terminal of the memristor circuit, as shown in Fig. 5, the charge of both memristors  $M_{s1}$  and  $M_{s4}$  increases while that of  $M_{s2}$  and  $M_{s3}$  decreases. Note that the polarities of memristors  $M_{s1}$  and  $M_{s4}$  are opposite from those of  $M_{s2}$  and  $M_{s3}$ . Accordingly, the magnitude of the resistances of memristors  $M_{s1}$  and  $M_{s4}$  decreases, while that of  $M_{s2}$  and  $M_{s3}$  increases.

If the magnitude or the duration of the pulse is big enough, the memristance of memristors  $M_{s1}$  and  $M_{s4}$  will reach its minimum value, while that of  $M_{s2}$  and  $M_{s3}$  will attain its maximum value, thereby resulting in an on (low memristance) state for  $M_{s1}$  and  $M_{s4}$ , and an off (high memristance) state for  $M_{s2}$  and  $M_{s3}$ . Afterward, any current signal appearing at the input terminal passes mostly through  $M_{s1}$ ,  $M_w$  and  $M_{s4}$ . Consequently, a larger voltage is produced at terminal  $V+$  than that at terminal  $V-$  with a positive current  $i$ . In this case, memristor  $M_w$  functions as a positive weight thereafter. On the other hand, when a negative wide pulse is applied as shown in Fig. 5, the voltage appearing at terminals  $V+$  and  $V-$  will be opposite to that of the previous case. In this case, the value  $M_w$  functions as a negative weight thereafter.

### Weight Setting

After the sign setting operation, the memristance is set for the synaptic weight. A pulse with a smaller width in the range  $[0, 0.7ms]$  is applied in this case. The equivalent range of the memristance  $M_w$  is  $[116 \text{ Ohm}, 1K\text{Ohm}]$  in the  $TiO_2$  memristor model.



### D. Four-Memristors Bridge-Based Synapses

The bridge circuit consists of four identical  $\text{TiO}_2$  memristors and is able to perform positive, negative and zero synaptic weighting. When a positive or a negative pulse  $V_{in}$  is applied at the input, the memristance of each memristor  $M_1$ ,  $M_2$ ,  $M_3$  and  $M_4$  is changed depending upon its polarity. For instance, when a positive  $V_{in}$  is applied as input, the memristance of  $M_1$  and  $M_4$  (whose polarities are forward biased) will decrease whereas the memristance of  $M_2$  and  $M_3$  (whose polarities are reverse biased) will increase. It follows that the voltage  $V_A$  at node A (with respect to ground) becomes larger than the voltage  $V_B$  at node B for a positive input signal. In this case, the circuit produces a positive output voltage  $V_{out}$  representing

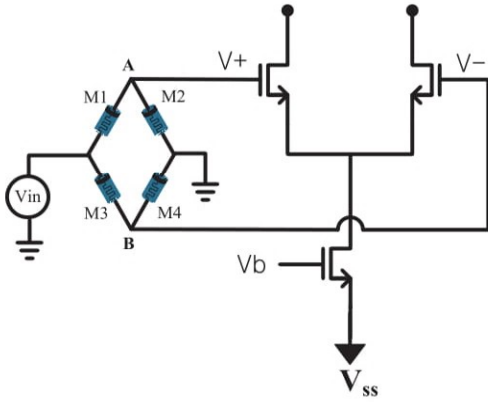


Fig. 6 Memristor bridge synaptic circuit.

a positive synaptic weight. On the other hand when a negative  $V_{in}$  is applied, the voltage at node B becomes larger than the voltage at node A and the circuit produces a negative output voltage  $V_{out}$  representing a negative synaptic weight. The voltage at different nodes in the circuit of Fig. 6 is given as

$$v_{M1} = \left( \frac{M_1}{M_1 + M_2} \right) v_{in} \quad (11)$$

$$v_{M2} = \left( \frac{M_2}{M_1 + M_2} \right) v_{in} = v_A \quad (12)$$

$$v_{M3} = \left( \frac{M_3}{M_3 + M_4} \right) v_{in} \quad (13)$$

$$v_{M4} = \left( \frac{M_4}{M_3 + M_4} \right) v_{in} = v_B \quad (14)$$

The required output is the voltage difference between terminal A and terminal B given as

$$v_{out} = v_A - v_B = \left( \frac{M_2}{M_1 + M_2} - \frac{M_4}{M_3 + M_4} \right) v_{in} \quad (15)$$

From Eq. (15) we see that the output voltage is equal to the input voltage weighted by a factor  $\psi$ , where

$$\psi = \left( \frac{M_2}{M_1 + M_2} - \frac{M_4}{M_3 + M_4} \right) \quad (16)$$

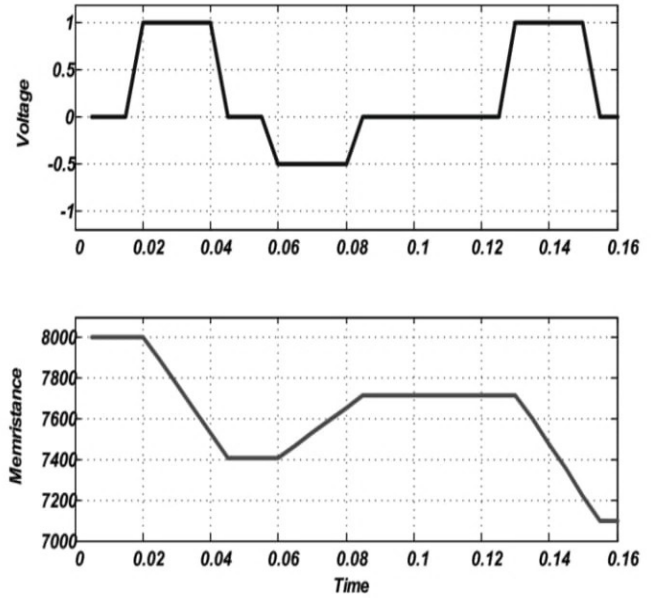


Fig. 7 Variation of Memristance of the  $\text{TiO}_2$  memristor by applying voltage signal.

The conditions for the bridge to function as weights in different regimes are listed as follow:

$$\frac{M_2}{M_1} > \frac{M_4}{M_3} \text{ Positive synaptic weight}$$

$$\frac{M_2}{M_1} < \frac{M_4}{M_3} \text{ Negative synaptic weight}$$

$$\frac{M_2}{M_1} = \frac{M_4}{M_3} \text{ Zero synaptic weight}$$

Each neuron must add a set of weighted input signals from diverse sources. This is implemented in the memristor bridge neuron via summing input signals with current mode circuits. The differential amplifier with three transistors in Fig. 6 is the voltage-to-current converter which functions as a current source.

### IV. Simulation Results

The memristance of the  $TiO_2$  memristor can be changed by applying appropriate current (or voltage) signal and the memductance remains unchanged whenever there is no external input as shown in Fig. 7.

Fig. 8 (a) shows the variation in memristance of the two  $TiO_2$  memristors M1 and M2 and Fig. 8 (b) shows the change in synaptic weight when a programming input voltage pulse  $V_{in}$  is applied to the circuit in Fig. 4. As can be seen from Fig. 8 (b), positive, negative and zero synaptic weighting can be performed with two anti-serial memristors as shown in Fig. 4. One possible implementation of memristor-based synapse that can emulate both positive and negative synaptic weights is shown in Fig. 8.

The five memristor synaptic circuit allows positive and negative weighting. The initial memristances  $Ms1=Ms4$  and  $Ms2=Ms3$  are assumed 15.98 KOhms and 116 Ohms, respectively. For the input current  $I$ , the voltage across  $M_w$  can be computed as  $-0.98 M_w \times I$ . Therefore, the initial sign of the weighting with the above memristances is negative. Fig. 9 shows the transition of the memristance at each memristor while a positive current pulse with +10mA amplitude is applied. At the end of the pulse, the memristances are turned into  $Ms1=Ms4=116$  Ohm and  $Ms2=Ms3=15.98$  KOhm.

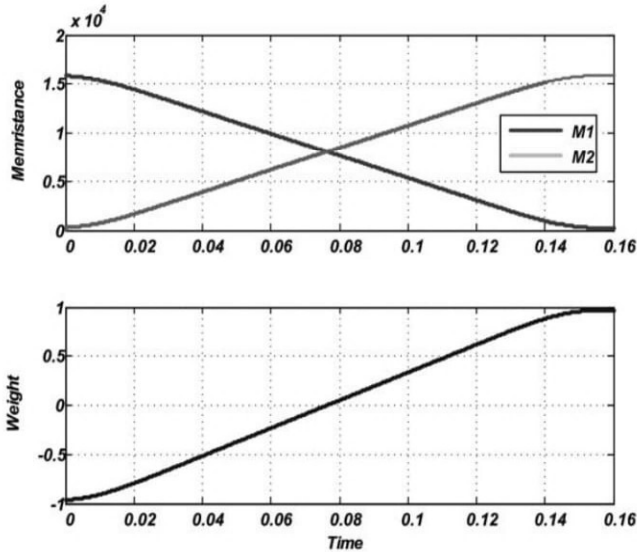


Fig. 8 Variation in memristance of the two  $TiO_2$  memristors and (b) the weight programmed when a voltage 1V is applied to the circuit.

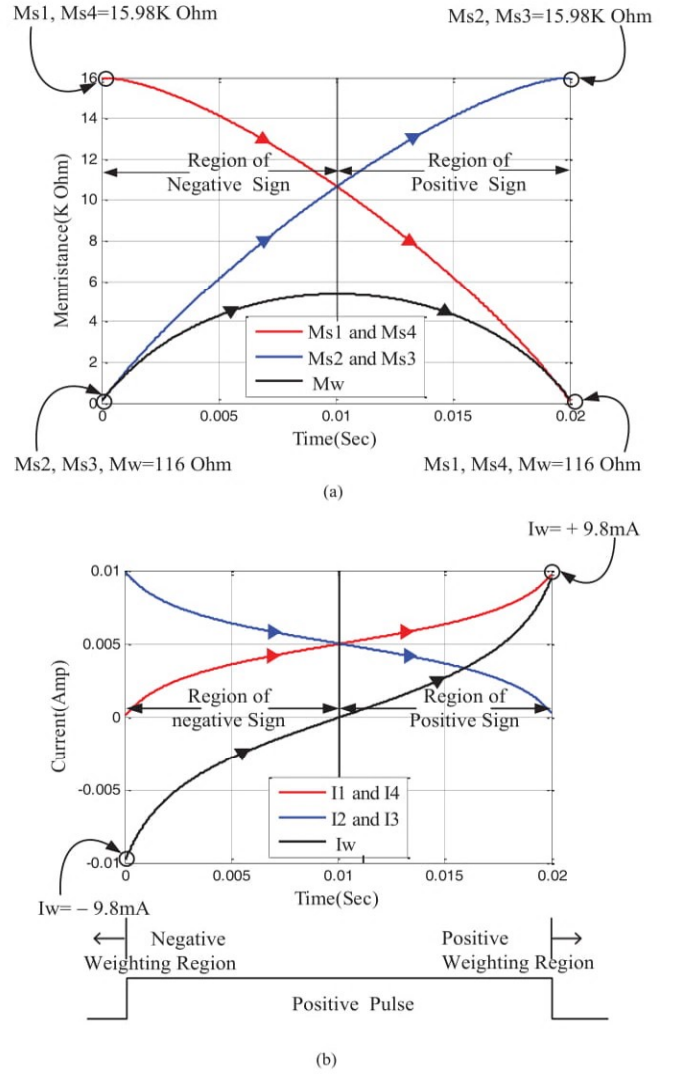


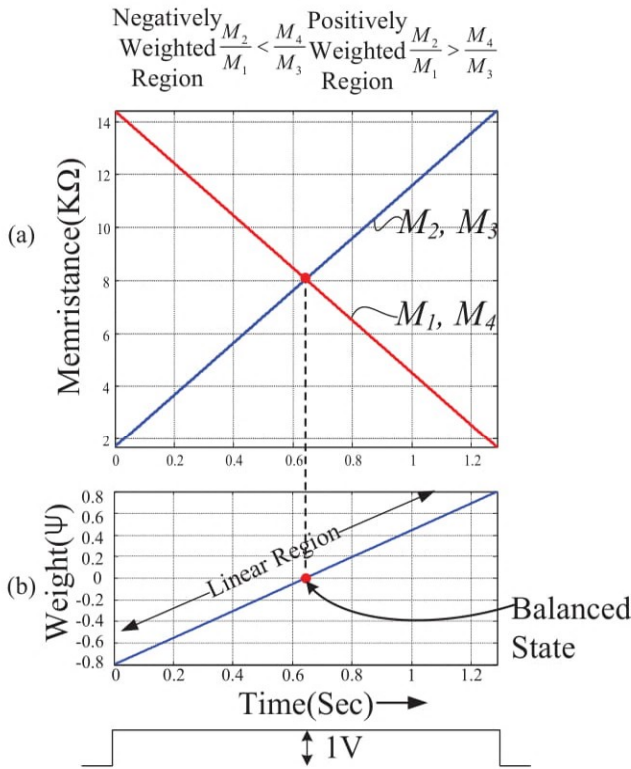
Fig. 9 (a) Memristance transition from  $\{Ms1=Ms4= 15.98$  K $\Omega$ ,  $Ms2=Ms3= 116$   $\Omega\}$  to  $\{Ms1=Ms4=116$   $\Omega$ ,  $Ms2=Ms3= 15.98$  K $\Omega\}$ . (b) Weight programmed.

Note that both the negative and positive signs can be obtained in the whole regions of the left and right side of Fig. 9, respectively. However, a shorter time is taken to program the same amount of memristance value in the two extreme state regions than in the middle regions. Similar to the positive sign transition as above, the negative sign can be implemented when a negative pulse is applied at a positive weighting state.

Fig. 10 shows the variation of memristance of the four memristors M1, M2, M3 and M4 and the corresponding synaptic weight realized when an input voltage  $V_{in}$  is applied to the circuit in Fig. 6. The bridge circuit can be used as synaptic weight in ANNs to realize positive, negative and zero weightings. Fig. 10



(a) shows the changes in the memristances  $M_1(t)$ ,  $M_2(t)$ ,  $M_3(t)$  and  $M_4(t)$  as a function of time, obtained via computer simulations of the memristor bridge circuit in Fig. 6 with initial memristances,  $M_1(0) = M_4(0) = 14.41 \text{ k}\Omega$ ,  $M_2(0) = M_3(0) = 1.69 \text{ k}\Omega$ . As shown in the figures, these numerically computed memristances in Fig. 10 (a) and the corresponding weight in Fig. 10 (b) are all very linear.



**Fig. 10 (a) Time variations of  $M_1(t)$ ,  $M_2(t)$ ,  $M_3(t)$ ,  $M_4(t)$ , and  $\psi(t)$  with memristor bridge circuit when a wide pulse is applied. The linear memristor model is assumed. (b) weight  $\psi(t)$ .**

### V. Comparison of the four Synapse Structures

Different pulse-based programmable memristor circuits for neural network applications are compared. The single memristor synapse is the simplest of all the four structures of memristor synapses discussed above. Since the conductance of memristor is directly used as analogous to synaptic weight, the output voltage across the memristor (or current through it) can be used directly to feed to the succeeding modules in the neural learning circuit. The two-terminal structure of the memristor can easily be integrated with the rest of

the neural learning circuit. Though simple in structure and easy to implement, the single memristor synapse has severe limitations in application due to the inability of implementing zero and negative synaptic weighting directly using conductance.

Whereas the two-memristor synapse and the memristor bridge synapse utilize the difference of voltage at different nodes in their structure to realize synaptic weights. Hence auxiliary circuits are required to make the output usable for succeeding layers when used in neural learning circuit. The two-memristor synapse however requires relatively more number of CMOS components in the auxiliary circuit than the four memristor bridge synapse. CMOS components occupy almost three orders of magnitude more chip area than a memristor. Therefore, more CMOS components means more chip area utilization.

The two memristor synapse and the five and four memristor bridge synapse however can implement positive, negative and zero weighting and have no restriction in applications and are particularly useful for applications where the weights are not known theoretically.

The single memristor synapse is particularly not suitable for implementing ANN rules like Back Propagation where the synaptic weights are not known a-priori and the weights can evolve either as positive or negative weights during learning.

The architecture of the five memristor bridge circuit is able to perform signed synaptic operations. However, it is very difficult to program small weighting near to zero. Moreover, a sign setting has to be performed before the weight setting of the input signal. The memristance of the switching memristors are also affected during the weight setting.

Also, a bridge synaptic circuit with four memristors, which is even simpler and efficient than five memristor based synaptic circuit. It is composed of four identical memristors that is able to perform zero, negative and positive synaptic weightings. Together with three additional transistors, the memristor circuit bridge weighting circuit is able to perform synaptic operation like an artificial neural cell. The memristor bridge based circuit has linear output characteristic compared to the conventional CMOS based Gilbert multiplier.

## VI. Conclusion

The non-volatile property and nano-dimension of memristor makes it a suitable component to be used as synapse for realization of simple and dense neural learning circuits. Use of conductance of a single memristor, analogous to the synaptic strength, is the simplest way to realize synapse in neural circuits. However, it can be applied only as positive weights. Combination of different memristors in a circuit can be utilized as synapse capable of performing positive, negative and zero weighting, like the two-memristor synapse and the memristor bridge-based synapse. But these structures require additional circuitry to extract the useful output which when realized with CMOS circuitry occupy greater chip area. Five memristor based synapses showed positive, negative and zero weighting, however, it shows the nonlinearity. Comparatively, the memristor bridge-based synapse requires less number of CMOS components than the two-memristor synapse and this makes the memristor bridge-synapse a better choice for implementing synapse in neural learning circuits.

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