THE OPTIMAL PLACEMENT OF A PHOTOVOLTAIC-INTEGRATED DYNAMIC VOLTAGE RESTORER FOR THE ENHANCEMENT OF POWER QUALITY WITHIN THE DISTRIBUTION SYSTEM: A CASE STUDY OF 11KV SIMARA INDUSTRIAL FEEDER IN NEPAL

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Abstract

Power Quality (PQ) issues like voltage sag, swell, and harmonics in electric power systems, especially those with an unbalanced radial network structure, dynamic compensation mechanisms are essential, particularly for industrial loads susceptible to voltage fluctuations due to faults or overloads. Dynamic Voltage Restorers (DVRs) have been proposed as a viable solution. However, when integrated into a distributed network, it becomes crucial to determine the optimal placement to maximize system performance. This paper focuses on a Photovoltaic (PV) system integrated DVR using Space Vector Transformation (SVT) with a Proportional Resonant (PR) Controller Control strategy. The primary objective is to minimize the System Average RMS Variation Frequency Index (SARFI) within the system of interest by identifying the optimal location of DVR. To assess the effectiveness of the proposed scheme, a functional PV-DVR model was developed using the MATLAB2023a/SIMULINK simulation environment. This model was implemented to dynamically restore node voltages to their pre-fault conditions in response to faults or overloads. The simulation results are presented for both an IEEE 13-node test distribution system and a 50-node typical radial industrial distribution system operating in Nepal. These simulation results serve to demonstrate the effectiveness and practicality of the proposed approach in mitigating power quality issues within electric distribution systems, thereby ensuring uninterrupted operation for critical industrial loads.

Keywords: *Power Quality (PQ), Photovoltaic (PV) system, Space Vector Transformation (SVT), Proportional Resonant (PR) Controller, System Average RMS Variation Frequency Index (SARFI),voltage profile, power loss, optimization.*

1. INTRODUCTION

Dynamic voltage restorers (DVRs) have been extensively studied in the literature as a good solution to reduce voltage disturbances in power systems. Voltage dips, surges and interruptions can cause serious damage to electrical equipment and disrupt the functioning of critical facilities such as data centers, hospitals and factories [2]. DVR is a power-based device that is balanced with the equipment to compensate for the voltage difference and control the power supply within the allowable range.

DVR design involves selecting the appropriate transducer topology, selecting the ratings of the transducer components, and deciding on the control strategy. Various converter topologies have been proposed such as voltage source converter (VSC), current source converter (CSC) and hybrid converter. VSC topology has become the most widely used switching topology in DVR due to its high power density, fast response and easy control [15]. Consideration of switching devices such as DC link capacitors [17], inductors, and semiconductor devices is another important consideration in DVR design. The rating of these items affects the price, size, and performance of the DVR.

There are several studies evaluating the performance of DVRs under different operating conditions, including various load impedances, fault locations, and fault types. Many studies have demonstrated the effectiveness of DVRs in compensating for voltage dips, swells, and outages. Also, Many control concepts have been proposed for DVR, such as PI control, fuzzy logic control, and model predictive control (MPC), Artificial Neural Networks [23].

A photovoltaic-based Dynamic Voltage Restorer (DVR) is a device that uses solar panels to provide power to the grid during voltage dips or spikes. The system combines two technologies: DVR and photovoltaic (PV) technology, offering a sustainable and environmentally friendly way to increase energy efficiency. The main purpose of photovoltaic-based DVR is to protect sensitive loads from voltage drops and maintain the voltage at a constant level. This is an ideal solution for rural areas where electricity is poor and the grid is weak. In recent years, many researchers have worked to improve the performance of PV-based DVR. Recent developments and research on photovoltaic-based DVRs have shown great results in reducing voltage drop and restoring voltage to pre-fault state.

The proposed PV-based DVR system uses a hybrid MPPT algorithm (Incremental Conductance and Integral Regulator) to improve performance. The proposed system has been tested on MATLAB Simulink and the results have shown that the system can reduce voltage dips/swells and provide a stable voltage to the load. The study found that space vector pulse width modulation (SVT) with PR controller [31] is effective in reducing voltage drop and stabilizing the load voltage. The proposed process also reduces THD and increases the power factor of the system.

The proposed system was tested on a standard IEEE 13-node distribution test system and 11kV Simara industrial distribution feeder in Nepal using novel optimization technique involving minimization of the System Average RMS Variation Frequency Index (SARFI) [24] within the system of interest by identifying the optimal locations PV-DVRs . According to the research results, photovoltaic integrated DVR can ensure the uninterrupted operation of the main enterprise by reducing the quality of electrical problems in the power distribution system.

2. PROPOSED DVR CONTROL SCHEME AND MOBELLING

The DVR system utilizes a series injection transformer, VSI, solar-based DC link, and control circuit for the purpose of retaining the base-phase voltage. The reference voltage waveform is used to compare the actual voltage pattern of the distribution system at the point of common coupling (PCC) to the voltage difference required by the DVR system. This difference is then adjusted by the Voltage Source Inverter (VSI) to provide the required power for the distribution system. The DVR inverter utilizes PWM technology to control the amplitude and phase angle of the voltage product, while the solar coupling system supplies the necessary reactive power for stable output. The SVT regulation minimizes power loss and ensures efficient power distribution, calculating the reactive power and reducing the loss on the load side as per the feedback from the PWM. The block diagram of proposed control scheme is shown in Fig 1.

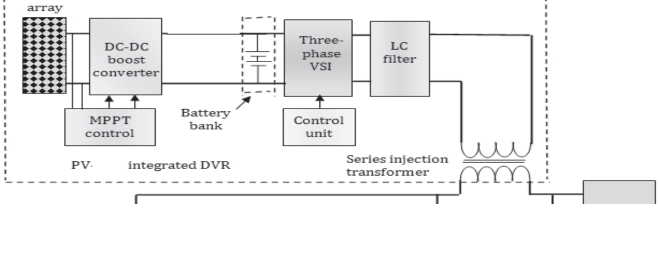


Fig. 1. Proposed Integrated DVR system.

2.1 MODELLING OF DVR

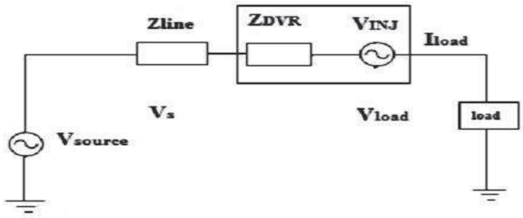


Fig. 2. Equivalent Circuit Diagram of DVR

The system impedance Z_{th} depends on the fault level of the load bus. When the system voltage (Vth) drops, the DVR injects a series voltage V_{DVR} through the injection transformer so that the desired load voltage magnitude V_L can be maintained. The series injected voltage of the DVR can be written as

$$V_{DVR} = V_L + Z_{th} I_L - V_{th} \quad \text{..................(1)}$$

Where,

V_L: The desired load voltage magnitude

Z_{th}: The load impedance.

I_L: The load current.

V_{th}: The system voltage during fault condition

The function of the DVR is to maintain the voltage by adjusting the magnitude, form, and phase of the voltage. By injecting the right amount of energy into the line, the DVR eliminates fluctuations in the voltage. In this approach, only the magnitude of the voltage was adjusted, with the load voltage assumed to be in phase with the pre-sag voltage. The load voltage and the reference voltage are fed into the controller, which then produces pulses to the inverter using the Pulse Width Modulation (PWM) approach, depending on the difference between the two voltages. Through the voltage injection transformer, the inverter injects the corresponding amount of energy into the line. This method is based on power quality enhancement for a grid system through the usage of a DVR powered by solar energy. This mainly reduces the sag and swell voltages.

The proposed methodology utilizes a Proportional Resonant Controller (PR), based on Space Vector Transformation (SVT) to effectively control the inverter voltage for synchronizing the line voltage and to reduce the harmonics on the load side. The PR controller has the highest gain at the desired frequency of the alternating voltage or current wave harmonic deviation. However, the harmonic compensators of the PR controller are restricted to a few low-current harmonics and the frequency of compensation is outside the control loop compensation. To obtain control over a wider loop bandwidth, a large proportion of the control loop gain can be chosen. For this efficient control system, the sag and swell voltages are neglected, and the system's harmonics are reduced. The Space Vector Transformation (SVT) is used to control PWM in the DVR inverter with a solar PV system, thus producing a synchronous output in the Distribution line.

2.2 SPACE VECTOR PULSE WIDTH MODULATION

Space vector modulation (SVM) is an algorithm used for the control of pulse-width modulation (PWM) in order to create alternating current (AC) waveforms, most commonly to drive 3 phase AC powered motors from DC using multiple class-D amplifiers. Variations of SVM can result in different quality and computational requirements, with one active area of development being the reduction of total harmonic distortion (THD) created by the rapid switching inherent to these algorithms.

A three-phase inverter converts a DC supply, via a series of switches, to three output legs which could be connected to a three-phase motor. The switches must be controlled so that at no time are both switches in the same leg turned on or else the DC supply would be shorted. This requirement may be met by the complementary operation of the switches within a leg i.e. if A+ is on then A− is off and vice versa, resulting in eight possible switching vectors for the inverter, V0 through V7 with six active switching vectors and two zero vectors (Table 1).

Vector	A^+	B^+	C^+	A^-	B^-	C^-	V_{AB}	V_{BC}	V_{CA}	
V_0 = {000}	OFF	OFF	OFF	ON	ON	ON	0	0	0	zero vector
V_1 = {100}	ON	OFF	OFF	OFF	ON	ON	$+V_{dc}$	0	$-V_{dc}$	active vector
V_2 = {110}	ON	ON	OFF	OFF	OFF	ON	0	$+V_{dc}$	$-V_{dc}$	active vector
V_3 = {010}	OFF	ON	OFF	ON	OFF	ON	$-V_{dc}$	$+V_{dc}$	0	active vector
V_4 = {011}	OFF	ON	ON	ON	OFF	OFF	$-V_{dc}$	0	$+V_{dc}$	active vector
V_5 = {001}	OFF	OFF	ON	ON	ON	OFF	0	$-V_{dc}$	$+V_{dc}$	active vector
V_6 = {101}	ON	OFF	ON	OFF	ON	OFF	$+V_{dc}$	$-V_{dc}$	0	active vector
V_7 = {111}	ON	ON	ON	OFF	OFF	OFF	0	0	0	zero vector

Table.1 Switching Vectors of SVT

To implement space vector modulation, a reference signal Vref is sampled with a frequency fs (Ts = 1/fs). The reference signal may be generated from three separate phase references using the αβγ transform. The reference vector is then synthesized using a combination of the two adjacent active switching vectors and one or both of the zero vectors. Different strategies for selecting the order of the vectors and which zero vector(s) to use exist, which will affect the harmonic content and the switching losses.

2.3 PR CONTROLLER

In comparison to traditional schemes, the Proportional-Resonant (PR) controller has been known to achieve improved frequency domain stability, superior current tracking behavior, and lower Total Harmonic Distortion (THD) in the proposed strategy. An ideal PR controller can be mathematically attained by converting an ideal synchronous frame PI controller to a stationary frame, with an open loop transfer function, $G_C(s)$, that has an infinite gain at the resonant frequency, ω0 (equation 2)

$$G_C(s) = K_p + \frac{2K_i s}{s^2 + \omega_0^2} \quad \text{........(2)}$$

Where,

ω0=Resonant Frequency

Kp= Proportional Gain

Ki= Integral Gain

$S^2 + \omega_0^2$= produces infinite gain at reference frequency

The term Ki is used to define various aspects of system dynamics, such as bandwidth, phase, gain margins, and more. A low value of Ki indicates a narrow bandwidth, while a large Ki implies a wider bandwidth. However, the use of a Proportional-Resonant (PR) controller with an infinite gain can lead to an infinite quality factor, which is not practical in real-world applications. To address this limitation, damping is introduced into an approximate non-ideal PR controller, as shown in Equation 3.

$$G_C(s) = G_{Cp}(s) + G_{Cr}(s) = K_p + \frac{2K_i\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \quad .....(3)$$

This damping factor helps specify the bandwidth around the resonant frequency, denoted as ω0, as ωc. In cases where voltage is introduced to the power line, voltage mismatches can occur due to the lack of synchronization in voltage waveforms. If the magnitude of the mismatched voltage increases, it results in an increase in line current, and conversely, a decrease in the mismatch voltage magnitude leads to a decrease in line current. Consequently, the amplitude of the mismatch voltage has a direct impact on the line current and, consequently, on the power obtained from the energy source.

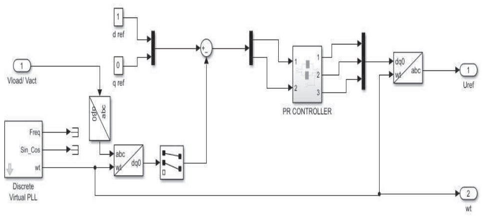


Fig. 3.Proposed Control Scheme in MATLAB.

3. OPTIMAL PLACEMENT OF PV INTEGRATED DVR

3.1 DESCRIPTION OF TEST SYSTEM

Case Study-1: IEEE 13 Node Test Distribution System

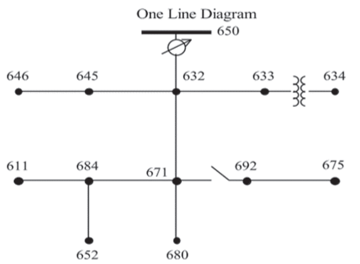


Fig. 4: IEEE 13 Node Test Distribution System

The IEEE 13 Node Test System, also known as the IEEE 13 Bus Test System, is a commonly used power distribution system test case in the field of electrical engineering and power systems analysis. It serves as a benchmark system for various studies, simulations, and research related to power distribution and grid analysis. This system represents a simplified but realistic model of a portion of an electrical distribution network. It is a 4.16kV/0.48kV, 60Hz, 3582kW, 1746KVAR system with overhead and underground lines with 1 regulator, one distribution transformer and one circuit breaker.

Case Study-2: 11kV Simara Industrial Feeder, Nepal

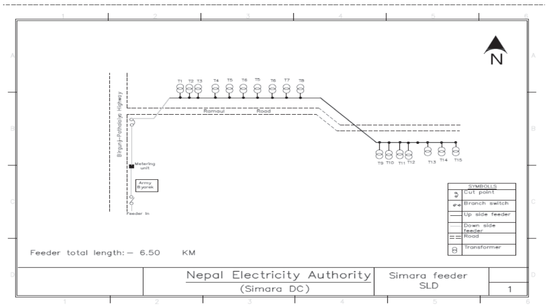


Fig. 5: 11/0.4kV Simara Industrial Feeder,Nepal

The 11kV Simara Industrial feeder, situated in Bara District within the jurisdiction of Simara DCs, Madesh Province, Nepal, encompasses a 6.5km stretch with all Dog Conductor, spanning from 132/11 Parwanipur S/S to the line section of last Industrial load Nepal Ceramics. This feeder comprises of only 15 industrial private 11/0.4kV transformers, with a collective installed capacity of 14.07MVA. This feeder is 50 node feeder with 35 11kV buses and 15 load buses.

Notably, it's important to recognize that all connected loads do not operate simultaneously during peak load periods. The feeder's load capacity, with a capacity of approximately 5.71MVA on a Dog Conductor, accommodates a peak loading of 300A. Under normal operating conditions, data gathered from each Time-of-Day (TOD) meter of the connected loads reveals a simulated load demand of 1.66MVA(at one of the instances). Under one of the operating conditions, data gathered from each Time-of-Day (TOD) meter of the connected loads reveals a simulated load demand of 5.955MV, which is load of 312A on the feeder. The relay for the feeder has an overload setting of 320A.

Table.2 Installed Transformer Capacity of Simara Feeder

S.N.	Location	Capacity (KVA)
1	Shiv shakti oil and fats	320
2	Shiv shakti agri	700
3	Rajesh metal	4600
4	B.G. Cotton	50
5	Krishna steels	850
6	Shubha laxmi metal	600
7	Harsa plastic	110
8	Gorkha feed	800
9	Narayani food product	500
10	RMC cement	1750
11	Win win metal Industries	300
12	Josis Gyavin	196.25
13	Nepal stonex	550
14	Nepal ceramic	1250
15	RMC food	1500
Total		14076.25

3.2 OPTIMIZATION IN THE TEST SYSTEM

Optimal location was determined with the objective of minimization of System Average RMS Frequency Index (SARFI) of the system in the presence of DVR. The objective is given by,

$$SARFI_X = \frac{\sum_{i=1}^{n} n_i x}{n} \quad .....(4)$$

Where,

X=RMS voltage threshold

$n_i x$=number of voltage sags lower than the specified threshold

n= total number of connected loads (with all the buses) .

The objective function is then given by,

$$y = \min\left(SARFI_X\right) = min\left(\frac{\sum_{i=1}^{n} n_i . x}{n}\right) \quad ....(5)$$

The sag threshold X is considered as 0.9 or 90% and swell threshold is considered 1.1pu or 110%, which indicates that we compute the system average sag frequency based on the number of buses whose voltages go below 90% and go above 110% of the nominal threshold value during a fault.

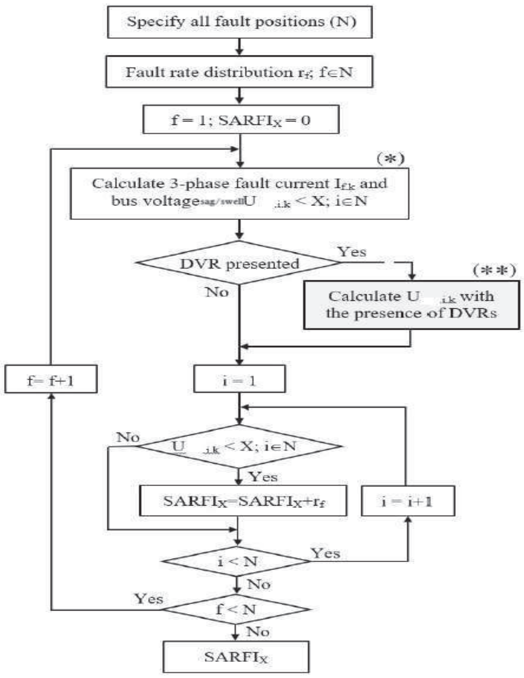


Fig 6: Flowchart for Calculation of SARFI

3.3 METHODOLOGY

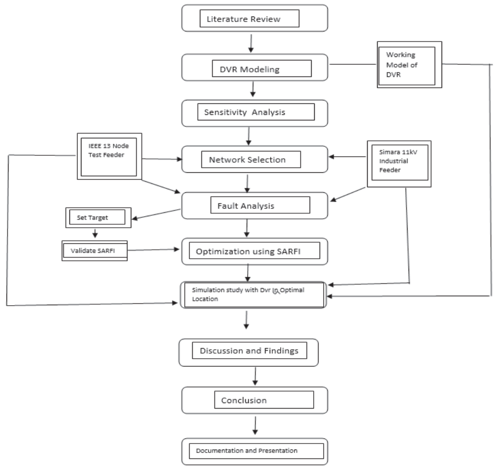


Fig 7 Flowchart for the proposed Methodology

The simulation models for both test systems were meticulously developed using MATLAB 2023a/SIMULINK software. These models underwent thorough analysis through short-circuit studies, followed by time-domain simulations. The objective was to evaluate the per unit (p.u.) three-phase voltages at all load buses within the network under various types of short circuits, including single line to ground (L-G), line to line (L-L), double line to ground (L-L-G), and balanced three-phase (L-L-L-G) faults. This analysis was conducted over a 0.1-second duration.

The collected post-fault voltages were treated as input data, while the nominal p.u. voltages at different buses served as the target output data. Specifically, the focus was on assessing the System Average RMS Frequency Index (SAFRI) for different bus voltage deviations from their respective target values. SAFRI offers insights into identifying the most vulnerable bus within the system, based on the highest voltage deviation from the target due to fault and due to overload in case of 11kV Simara feeder. Subsequently, the bus exhibiting the most significant deviation from the target voltage was identified as the optimal location for the placement of a Dynamic Voltage Restorer (DVR). This approach ensures that the DVR is strategically positioned to effectively mitigate voltage deviations and safeguard the stability of the power system.

4. Results and Discussuions

4.1 VOLTAGE SAG,SWELL AND HARMONICS PROBLEM MITIGATION BY PV INTEGRATED DVR

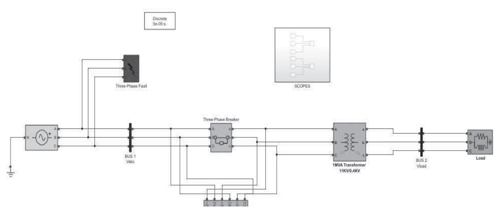


Fig 8: Proposed System Model in MATLAB

The investigation of the PV-integrated DVR model's response to various voltage disturbances was conducted through simulation. A three-phase balanced fault scenario was simulated, lasting for a duration of 0.1 seconds, occurring between t=0.2s and t=0.3s. This simulation aimed

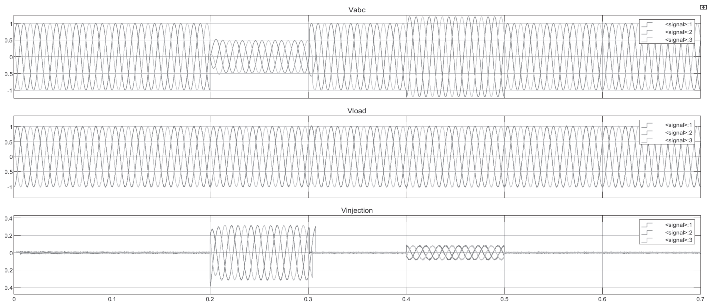


Fig 9: Load Voltage (DVR) for a 3-phase fault

to replicate a voltage sag across the load, resulting in the load voltage decreasing to 80% of its normal value, as illustrated in Figure 9 (Vabc) . Additionally, a voltage swell was emulated by externally injecting voltage using a programmable voltage source in MATLAB. This injection started at t=0.4s and continued until t=0.5s. During this period, the system's voltage increased to 120% of its nominal value. The system was then operated in the presence of PV integrated DVR in series with a distribution line feeding a load. Figure 4.1 (Vload) shows the events after the installation of the DVR. The first figure shows the source voltage during a fault (voltage sag, swell), the second figure shows that the load voltage after DVR has compensated the voltage sag and swell. It can be clearly observed that when the source voltage sags from t=0.2 to 0.3 s and swells from t= 0.4 to 0.5 s, DVR has either injected or absorbed the power for a constant voltage across the load terminal. The third figure (Vinjection) in Figure 9 shows the profile of power injection and absorption by the DVR. From the third figure, it can be seen that the DVR has injected voltage (power) into the load from t=0.2s to t=0.3s for voltage sag whereas, DVR has absorbed the excess voltage from t=0.4s to 0.5s for voltage swell. It is seen that the injected voltage by DVR, during sag/swell varies to bring back the load voltage.

It has been shown that the developed DVR model mitigates balanced voltage sags and swells occurring in the load, even when the source side voltage has sagged or swelled.

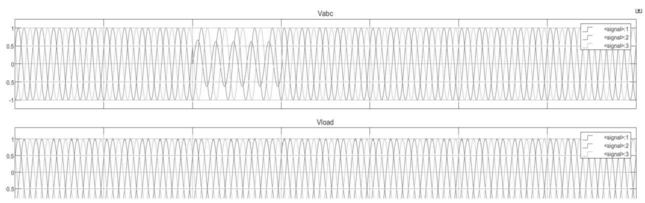


Fig 10: Load Voltage (DVR) for a SLG fault

Balanced faults are the least occurring events in power systems, with unbalanced fault unbalanced faults occurring for more than 95% of the time. Among different faults, Single Line to Ground (SLG) faults are the most frequent– responsible for almost 80% of the total number of faults. It is important that the modeled DVR is able to compensate for the unbalanced voltage sags during SLG faults occurring in the systems.

For this, an unbalanced fault (SLG) fault has been simulated for the time duration of 0.2 s to 0.3 s, Waveforms of load voltage under this unbalanced fault show that Phase A has decreased to 10% of its normal operating voltage while the phases B and C and still healthy in Figure 8. It can be clearly observed that when the source voltage sags from t=0.2 to 0.3 in Phase A. DVR has injected voltage for phase A.

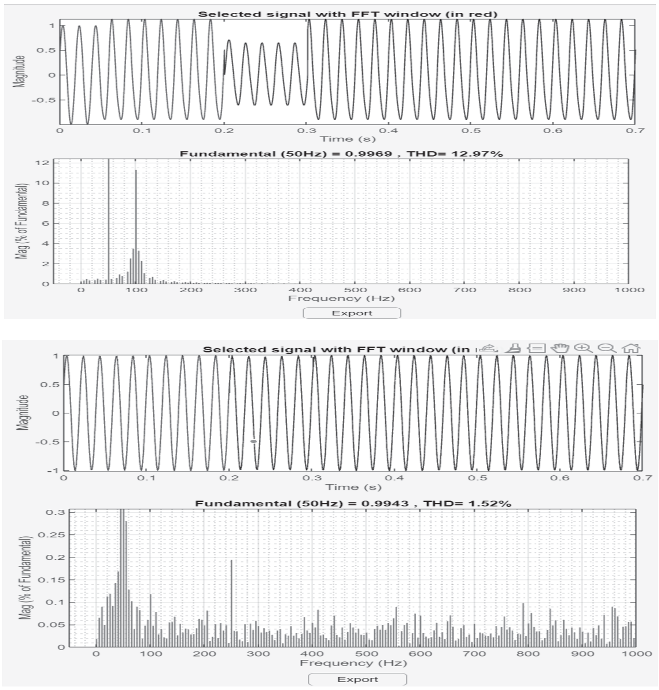


Fig 11: Harmonics of the System before and after Installation of DVR in model test system during fault

PV integrated DVR with space Vector Pulse with Modulation with PR Controller was also able to decrease the THD during balanced three phase fault from 12.97% to 1.52% when fed with 3rd Harmonics in the system by programmable Voltage Source in MATLAB .

4.2 CASE STUDY 1:IEEE 13 NODE TEST DISTRIBUTION SYSTEM

IEEE 13 Node Test Distribution Feeder have been modeled in MATLAB/SIMULINK environment, and the same model has been simulated for different faults scenario and the values of the post fault voltages were measured and were used for SAFRI Calculation for Optimal Location of PV-Integrated DVR.

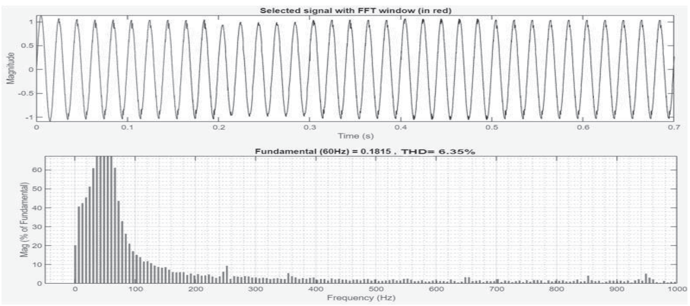
Following the procedure of optimization, it was observed that at node 633(i.e. between branch (632-633) lowest value of SARFI 6.66 among the three-phase bus was observed. Then DVR was placed in the node to observe the performance. As was the most vulnerable node. Table 2 shows the SAFRI values of all the three phase buses of the system.

Location (BUS)	$SAFRI_X$ VALUES
632	7.14
633	**6.66**
643	7.69
650	11.11
675	6.67
680	7.14
692	10

Table.3 SAFRI Values IEEE 13 Node Test System

As a result, branch 632-633 , in IEEE 13 node system was chosen as the optimal location.

The maximum vulnerability of a node in the system can be attributed to its location in the system along with the load distribution such that for most of the faults in the system, the vulnerable bus lies in the fault current-carrying path as a result has maximum value for its voltage deviation from the rated voltage.



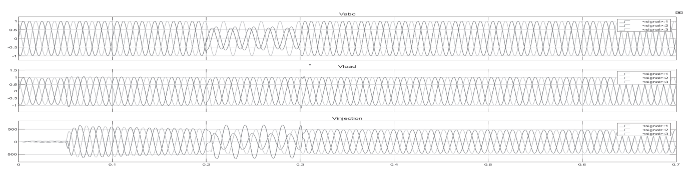


Fig 12: Load Voltage IEEE 13 node Test system for a LLG fault

It has been shown that the developed DVR model is able to mitigate unbalanced voltage sags (DLG Fault at node 632) between t=0.2s to 0.3s and swells between t=0.4s to 0.5s occurring in the load, even when the source side voltage has sagged to 60%. This model is tested in different radial distribution systems in different Fault conditions and Fault location, to effectively restore the voltages in the system buses under certain undesired events.

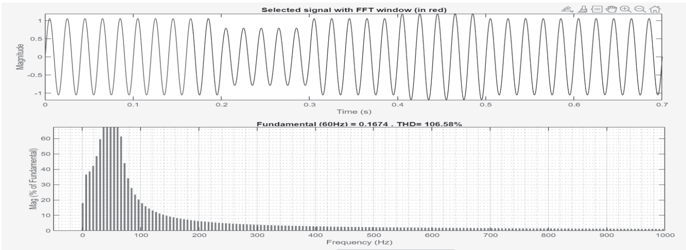


Fig 13: Harmonics of the System before and after Installation of DVR in IEEE 13 Node test system during fault

PV integrated DVR with space Vector Pulse with Modulation with PR Controller in IEEE 13 node Test System was also able to decrease the THD during balanced three phase fault from 106.58% to 6.35% in 60Hz System. Which is just slightly higher than threshold value of 5% but it is in acceptable range considering the complexity of IEEE 13 Node test distribution system.

4.3 CASE STUDY 2: 11KV SIMARA INDUSTRIAL FEEDER-NORMAL LODAING CONDITIONS

The 11kV Simara Industrial Distribution Feeder has been modeled within the MATLAB/SIMULINK environment. This comprehensive model incorporates load data obtained from Time-of-Day (TOD) meters installed at all 15 consumer sites. It undergoes simulation for various fault scenarios, with post-fault voltage values meticulously recorded. These voltage measurements form a critical component for the subsequent calculation of the System Average Fault Ride Through Index (SAFRI), aiding in the identification of the optimal location for the PV-Integrated Dynamic Voltage Restorer (DVR).

Following the prescribed optimization procedure, the analysis revealed that the lowest SAFRI value, denoting superior voltage stability, was recorded at bus 5, situated between branches 4 and 5, with a SAFRI value of 8.2. Notably, the second lowest SAFRI value, at 9.11, was observed at bus 12, found between branches 11 and 12. Bus 12 also emerges as a significant consideration due to its vulnerability and high load capacity, hosting Rajesh Metal with an installed transformer capacity of 4600KVA. Ultimately, the decision was made to place the DVR at bus 5, recognized as the most optimal position, to closely monitor its performance. It was a prudent choice, particularly given bus 12's vulnerability. Figure 14 provides a visual representation of SAFRI values across all 11kVbuses within the system.

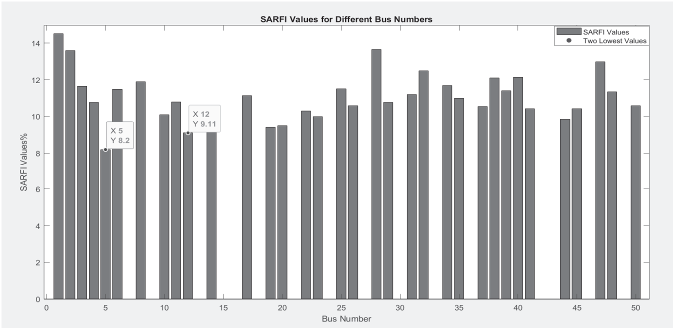


Fig 14: SAFRI values at different buses simara industrial feeder

As a result, branch 4-5, the section of 11 kV Simara Industrial feeder was chosen as the optimal location. A 6kV, PV system has been effectively deployed in a DVR (Dynamic Voltage Restorer) to successfully mitigate voltage sags and swells. Figure 15 illustrates the input and output characteristics of the branch housing the PV-DVR. A LL fault is deliberately induced at the system's most critical location, and the resulting perturbations are effectively mitigated. The PV-DVR demonstrates success in rectifying voltage sags and swells, bringing them in close proximity to the 1 per unit (p.u.) reference value. Additionally, it efficiently addresses sag, swell and harmonics problems in the system, even when subjected to various fault conditions.including Single Line-to-Ground (SLG), Line-to-Line-to-Line-to-Ground (LLLG), Line-to-Line-to-Line (LLL), and Line-to-Line (LL) faults.

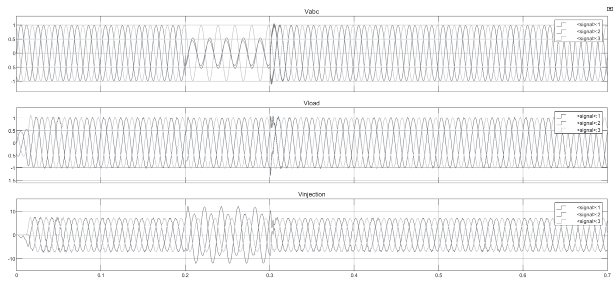


Fig 15: Input and output Voltages of installed PV-DVR in simara feeder in MATLAB

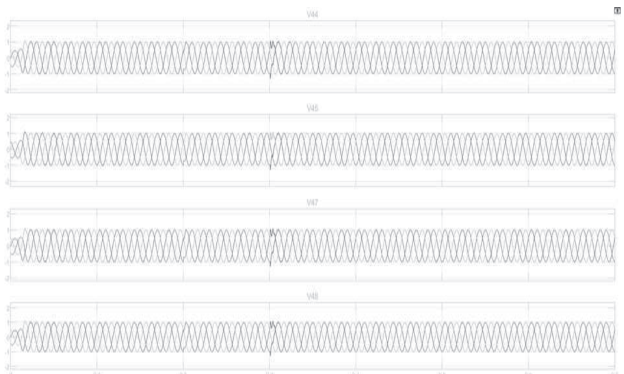


Fig 16: Output Voltages of the farthest 11kV buses after installation PV-DVR in simara feeder during LL fault

Fig 17: Output Voltages of the farthest 0.4Kv (load) buses after installation PV-DVR in simara feeder during LL fault

PV integrated DVR effectively compensates for the voltage fluctuations not only at nearest bus V5 but extends its support seamlessly to cover all buses up to the final 11kV bus, V50 (i.e nearly 0.98p.u.), during fault occurrences. Furthermore, this compensation encompasses all the load (0.4kV) buses within this network.

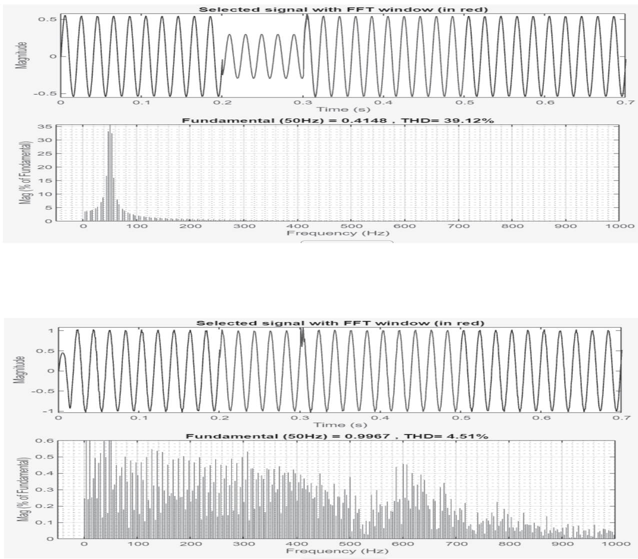


Fig 18: Harmonics of the System before and after Installation of DVR in 11kV Simara Feeder during Fault conditions

The integration of a Photovoltaic (PV) system into the Dynamic Voltage Restorer (DVR) system, utilizing Space Vector Pulse Width Modulation (SVPWM) with a Proportional-Resonant (PR) controller, represents a significant advancement in the management of power quality within the 11kV Simara Industrial feeder. Total Harmonic Distortion (THD) during line-to-line (LL) faults, condition spanning 25 cycles, commencing at t=0.2s and concluding at t=0.5s, within the 50Hz system, the DVR integrated system succeeded in reducing THD from an initially high 39.12% to as as low 4.51%.

4.4 CASE STUDY 2: 11KV SIMARA INDUSTRIAL FEEDER-HEAVY LODAING CONDITIONS

During peak load periods, it's clear that not all connected loads are in operation simultaneously. The feeder, with a capacity of approximately 5.71MVA on a Dog Conductor, can handle a peak load of 300A. However, under specific operating conditions, data from Time-of-Day (TOD) meters on connected loads indicate a simulated load demand of 5.955MVA (at one instance), equivalent to a 312A load on the feeder. The feeder's relay is set to trip at 320A. When the current reaches 312A, only buses 1, 2, and 3 maintain a voltage of 1 per unit (p.u.), while all buses beyond experience a voltage drop from 0.84 p.u. to 0.89 p.u., with the farthest bus being the most affected.

To address this voltage issue, a Dynamic Voltage Restorer (DVR) was optimally placed at the branch 4-5 section of the 11kV Simara Industrial feeder.

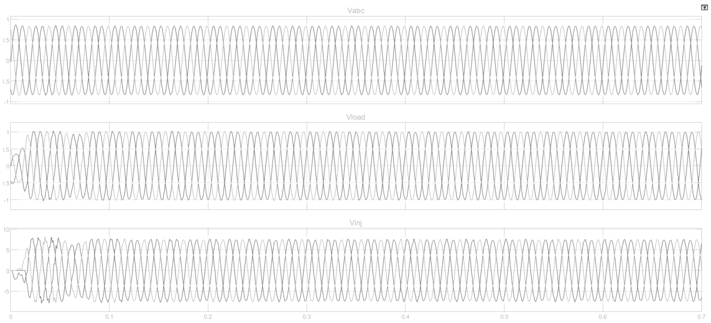


Fig 19: Input and output Voltages of installed PV-DVR in simara feeder in MATLAB in feeder overloaded conditions.

Figure 19 depicts the input and output characteristics of the branch housing the PV-DVR. During the feeder's overload condition, only buses V1, V2, and V3 manage to maintain their voltage close to 1 per unit (p.u.). However, following the strategic placement of the DVR, The DVR consistently maintains the voltage levels within the range of 0.95 p.u. to 0.99 p.u. across all 11kV buses and load buses, including the farthest 11kV buses, V47, V48, V50, and the farthest load bus, V49. This performance is illustrated in Figures 20 and 21.

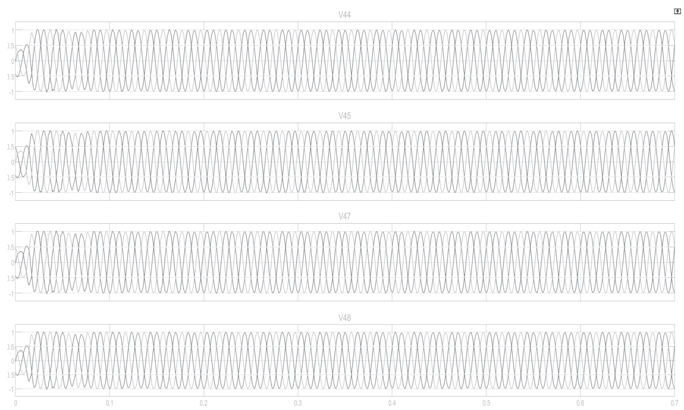


Fig 20: Output Voltages different 11kV buses after implementation of PV-DVR in simara feeder in feeder over-load conditions.

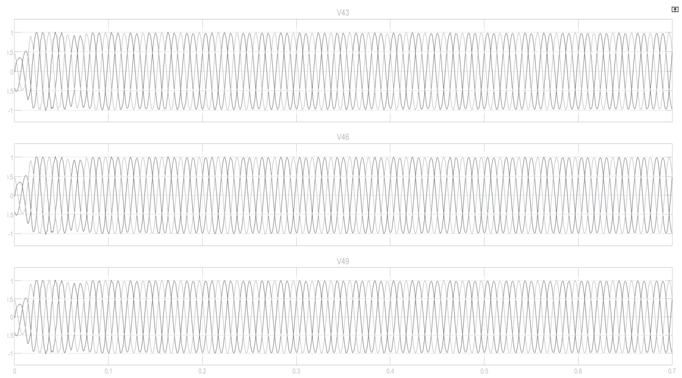


Fig 21: Output Voltages different load (0.4kV) buses after implementation of PV-DVR in simara feeder in feeder over-load conditions.

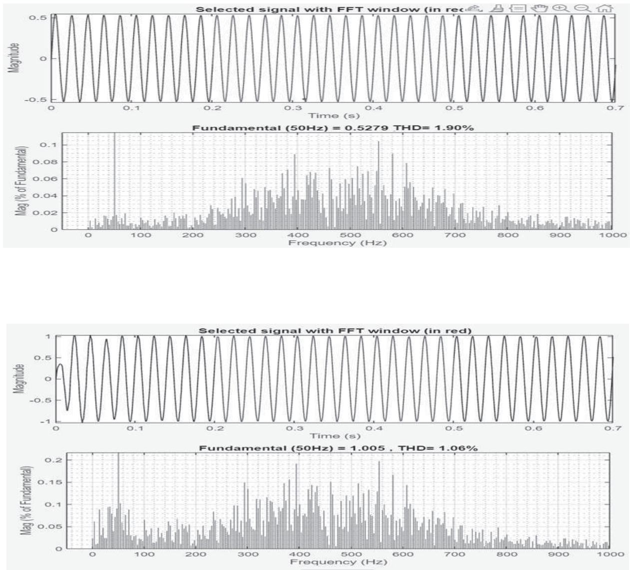


Fig 22: Harmonics of the System before and after Installation of DVR in 11kV Simara Feeder during overload conditions.

Proposed approach has yielded impressive results, particularly in mitigating Total Harmonic Distortion (THD) during feeder-overloaded conditions. Spanning 25 cycles, commencing at t=0.2s and concluding at t=0.5s, within the 50Hz system, the DVR integrated system succeeded in reducing THD from an initiaL 1.90% to lower 1.06%.

4. CONCLUSION

This study implemented a compensation model that integrates a Photovoltaic System with a Dynamic Voltage Restorer (DVR) and a Space Vector Pulse Width Modulation (SVT) based Proportional-Resonant (PR) controller. The purpose of this integrated system was to address grid power fluctuations in both the IEEE 13 Node Test Distribution system and the 11kV Simara Industrial feeder in Nepal. The SVT controller was employed to dynamically adjust the Pulse Width Modulation (PWM) of the inverter and utilize the DVR offset to generate the necessary reactive power, thereby ensuring power quality within the grid. The proposed PR control system offered the flexibility to align its individual resonant peaks with the grid frequency while injecting the compensated voltage using the DVR-based SVT system. An advantage of this approach was its lower computational overhead and the absence of a dedicated grid voltage feed-forward control path in the DVR system. For three-phase grid-connected systems, the PR technique effectively compensated for both positive and negative sequence components simultaneously, obviating the need for a synchronous reference frame. In contrast, a PI controller typically necessitates a synchronous reference frame to compensate for positive and negative sequence voltages.

The performance of the system utilizing the PR controller in conjunction with the DVR system surpassed that of conventional controllers. Notably, the Total Harmonic Distortion (THD) of the proposed system was exceptionally low, registering at just 1.06% during reactive power compensation in both the IEEE 13 node test distribution system and the 11kV Simara Industrial feeder in Nepal.

These results highlight the effectiveness of the integrated Photovoltaic-DVR system with SVT-based PR control in maintaining optimal power flow within the power supply and distribution systems. This approach not only enhances power quality but also contributes to stable and reliable energy distribution.

REFERENCE

[1] Nepal Electricity Authority. A year in review 2020/2021, 2021,2022

[2] Naeem Abas , (member, IEEE), Saad Dilshad , (graduate student member, IEEE), Adnan Khalid1, Muhammad Shoaib Saleem , and,Nasrullah Khan, (Senior Member, IEEE), Power Quality Improvement Using Dynamic Voltage Restorer,IEEE ,August 27,2020

[3] Zovnomir Klaic,Srete Nikoloslav,Zorislav Kraus,-Voltage Variation Performance Indices in Distribution Network,2018

[4] IEEE POWER ENGINEERING SOCIETY,IEEE 13 Node Test Feeder.

[5] Tiago Davi Curi Busarello; Jose Antenor Pomilio; Marcelo Godoy Simoes, Design Procedure for a Digital Proportional-Resonant Current Controller in a Grid Connected Inverter,2018

[6] M. H. J. Bollen, Understanding Power Quality Problems—Voltage Sags and Interruptions. New York, NY, USA: IEEE Press, 2000.

[7] A. Ghosh and G. Ledwich, Power Quality Enhancement Using Custom Power Devices.

[8] N.G. Hingorani and L Gyugyi, “Understanding FACTS – Concepts and Technology of Flexible AC Transmission Systems”, Wiley, 2000.

[9] R. C. Dugan, M. F. McGranaghan, and H. W. Beaty, Electric Power Systems Quality, 2nd edu. New York, NY, USA: McGraw-Hill, 2006.

[10] A. Moreno-Munoz, Power Quality: Mitigation Technologies in a Distributed Environment. London, U.K.: Springer-Verlag, 2007.

[11] K. R. Padiyar, FACTS Controllers in Transmission and Distribution. New Delhi, India: New Age Int., 2007.

[12] [12] IEEE Recommended Practices and Recommendations for Harmonics Control in Electric Power Systems, IEEE Std. 519, 1992.

[13] S. Middlekauff and E. Collins, “System and customer impact,” IEEE Trans. Power Del., vol. 13, no. 1, pp. 278–282, Jan. 1998.

[14] M. Vilathgamuwa, R. Purer, S. Choi, and K. Tseng, “Control of energy optimized dynamic voltage restorer,” in Proc. IEEE IECON, 1999, vol. 2, pp. 873–878.

[15] J. G. Nielsen, F. Blaabjerg, and N.Mohan, “Control strategies for dynamic voltage restorer compensating voltage sags with phase jump,” in Proc. IEEE APEC, 2001, vol. 2, pp. 1267–1273.

[16] A. Ghosh and G. Ledwich, “Compensation of distribution system voltage using DVR,” IEEE Trans. Power Del., vol. 17, no. 4, pp. 1030–1036, Oct. 2002.

[17] I.-Y. Chung, D.-J. Won, S.-Y. Park, S.-I. Moon, and J.-K. Park, “The DC link energy control method in dynamic voltage restorer system,” Int. J. Elect. Power Energy Syst., vol. 25, no. 7, pp. 525–531, Sep. 2003.

[18] E. C. Aeloíza, P. N. Enjeti, L. A. Morán, O. C. Montero-Hernandez, and S. Kim, “Analysis and design of a new voltage sag compensator for critical loads in electrical power distribution systems,” IEEE Trans. Ind. Appl., vol. 39, no. 4, pp. 1143–1150, Jul./Aug. 2003.

[19] J. W. Liu, S. S. Choi, and S. Chen, “Design of step dynamic voltage regulator for power quality enhancement,” IEEE Trans. Power Del., vol. 18, no. 4, pp. 1403–1409, Oct. 2003

[20] Villalva, Marcelo Gradella, and Jonas Rafael Gazoli. "Comprehensive approach to modeling and simulation of photovoltaic arrays." IEEE Trans. Power Electron. 24.5 (2009): 1198-1208.

[21] Altas, I. H., and A. M. Sharaf. "A photovoltaic array simulation model for matlab-simulink gui environment." International Conference on Clean Electrical Power, ICCEP, IEEE, 2007.

[22] Kawamura, Hajime, et al. "Simulation of I & V characteristics of a pv module with shaded pv cells." Solar Energy Materials and Solar Cells, vol.75, no.3, 2003, pp. 613-621

[23] Ghimire, A., Bhattarai, N. & Motra, L., 2020. Optimal placement of Dynamic Voltage Restorer in Radial Distribution System using Artificial Neural Network Approach. International Research Journal of Engineering and Technology (IRJET), May.07(05).

[24] Khanh Q. Bach, “A Novel Method For Global Voltage Sag Compensation In Ieee 69 Bus Distribution System By Dynamic Voltage Restorers” , 2019

[25] Hanju Cha; Trung-Kien Vu; Jae-Eon Kim, “Design and control of Proportional-Resonant controller based Photovoltaic power conditioning system”,IEEE Conference,2009

[26] Tiago Davi Curi Busarello, Design Procedure for a Digital Proportional-Resonant Current Controller in a Grid Connected Inverter, 4th IEEE Southern Power Electronics Conference, SPEC 2018

[27] Abdul Hameed Soomro , Abdul Sattar Larik , Mukhtiar Ahmed Mahar

[28] Anwer Ali Sahito , Amir Mahmood Soomro ,Ghulam Sarwar Kaloi,”Dynamic Voltage Restorer—A comprehensive review”,Energy Report 7 (2021)

[29] Zvonimir klaic,Srete Nikolovski ,Zorilav Kraus,” Voltage Variation Performance Indices in Distribution Network,ISSN

[30] Wei Du;Kevin P. Schneider;Greg P. Wiegand;Francis K. Tuffner;Jing Xie;Orris L.Dent, A Supplemental Control for Dynamic Voltage Restorers to Improve the Primary Frequency Response of Microgrids,IEEE Transactions on Smart Grid,2022

[31] Viswaprakash Babu 1, K. Shafeeque Ahmed1, Y. Mohamed Shuaib 1, (Member, Ieee), And M. Manikandan2, (Senior Member, Ieee), Power Quality Enhancement Using Dynamic Voltage Restorer (DVR)-Based Predictive Space Vector Transformation (PSVT) With Proportional Resonant (PR)-Controller,November 15,2021.