# Etching of Crystalline Silicon in Thermal Environment

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***Abstract***

*Thin wafer have become a basic need for a wide variety of new microelectronic products. Wafers that have been thinned using wet etch process on the backside have less stress compared with standard mechanical back grinding. Isotropic wet etching of silicon is typically done with a mixture of nitric and hydrofluoric acids. As the silicon is etched and incorporated in the etching solution the etch rate will decrease with time. This variation has been modeled. The focus of this paper is to compare the process control technique for maintaining a consistent etch rate as a function of time and wafer processed.*

***Keywords:*** *isotropic and anisotropic etching, MEMS, SOI, LPCVD.*

**Introduction**

Micro Electro Mechanical Systems (MEMS) is an integration of mechanical elements and electronic circuit on a common substrate through the use of microfabrication technique to achieve high performance devices with dimensions ranging from less than a micron to several microns. Most of the MEMS devices are currently based on silicon because of the available surface machining technology. Silicon, a MEMS material, has been chosen for investigation with particular emphasis in etching. Etching technology in thin film process plays an important role in the semiconductor industry. Isotopic/anisotropic etching of silicon is used to obtain varied microstructures. Anisotropic etching of silicon is extensively done by taking KOH solution as etchant. In semiconductor processing because of their low cost, high throughput, and excellent selectivity. Important progress in the fabrication of microelectrical structure with integrated circuits has been achieved by many researchers using KOH wet etching. Fabrication of UMOS transistors on Si (111) wafers for high power and high current densities has been achieved by applying KOH anisotropic wet etching to the silicon substrate [1–3]. Other applications include the fabrication of VMOSFETs, radio frequency amplifiers, power supplies and microcomputers [4]. Using its selective and anisotropic etching properties, KOH has been applied to yield devices snel as field emission devices, optical waveguides, pressure sensors and ink nozzles [5-9].

KOH etching is one of the oldest anisotropic orientation dependent wet etching technique. Etching of (100) oriented silicon using aqueous KOH creates V-shaped grooves with (111) planes at an angle of 54.74° from the (100) surface (or 35.3° from the normal) [4]. This etch process is independent of the doping concentration for As, P and Sb. KOH solution can also be used to produce mesa structures [3]. There are several models proposed for the silicon etching mechanism in aqueous KOH. Bean and Runyan [10] found that the slow etch rate in the (111) direction is a consequence of the diamond lattice structure because the (111) plane is a double layer bound together by more atomic bonds than other planes. Glembocki *et al.* proposed an electrochemical reaction mechanism that exists in the rate determining step for KOH etching [9-10]. A compromise model was proposed by Seidel *et al.* in 1990 assuming that electrochemical reactions dominate during etching and that anisotropic etching was caused by the orientation-dependent number of dangling bonds available per surface area. The (100) Si surface etches faster than the (111) because the free surface of (100) Si is attacked by one $OH^-$ per Si atom, whereas the (111) Si surface is attacked by two $OH^-$ per Si atoms. Although the mechanisms are not clear, it is known that electrochemical reactions play an important role in this process [9]. Hence, etching of single crystal silicon in aqueous KOH is of both technological and fundamental importance.

It is clear from above discussion that applications of anisotropic KOH etching of silicon for the fabraication of MEMS parts is mostly based on the angular dependence of etch rates (ER), creating

thin diaphragms. Taking this into account, paper is focused on to demonstrate absolute values of orientation dependent etch rate (i.e., ER anisotropy) changes with temperature and tried to understand basic mechanism behind it.

**Experimental Procedure**

The development of method for the production of miniaturized mechanical components and devices with Si is a natural outgrowth of Si surface machining methods have been developed for the production of microcircuits. Proceed towards this direction, we prepare fresh KOH solution by weighing 1 part KOH pellets into a plastic beaker and then add 2 parts of DI water. As an example, use 100 g KOH with 200 ml water. Mix on warm surface until KOH has dissolved. Add 40 ml of isopropyl alcohol to the solution. The isopropyl alcohol increases the anisotropy in etching. The KOH etch requires a "hard mask" of silicon dioxide or silicon nitride (nitride is preferred since oxide is slowly etched by KOH). The details on making a hard mask can be found elsewhere [4-6]. The basic approach is as follows. Start with silicon (100) polished wafer. Clean wafers and pattern with photoresist. Use the reactive ion etches (RIE) system to etch the exposed oxide or nitride surface, for oxides: $CHF_3$ and $O_2$ or $CF_4$ and $O_2$. Etch until the silicon is exposed (shiny); typically 5 minutes per 1000 Å film. Rinse the wafer with acetone to remove the remaining photoresist. Rinse with DI water, and then blow dry. Put KOH solution in glass container and warm to 80° C on a hot plate. If desired, use a mixer to agitate the solution. Place patterned wafer (with patterned hard mask) in the KOH solution. The KOH will bubble at the exposed silicon sites while etching occurs. The etch rate for 30% KOH at 80°C should be about 1 micron/minute. Rinse all labware three times in clean water. In very small amounts (less than 30 ml): Dilute the KOH with cold water, then neutralize with a small amount of HCl. If the pH is below 12.5, pour the solution down the drain, flushing with plenty of cold water.

The wafer used in this study was thermally bonded silicon on insulator (SOI) wafer with (100) orientation. The thickness of the top Si, buried $SiO_2$ layer and bottom Si. The wafers are of *p*-type. Only the top Si layer was etched by the KOH solution. First of all, the SOI wafers are prepared with standard RCA cleaning. A 450 Å layer of $Si_3N_4$, which acts as a KOH etching mask, deposited on each wafer using low pressure chemical vapor deposition (LPCVD). Oxide can be used as an etch mask for short periods in the KOH solution. For long periods, nitride is a better etch mask as it etches more slowly. The SOI wafer then cut into 5mm × 5mm pieces. With the diced pieces, positive photoresist, will be used to pattern the $Si_3N_4$ for the KOH etching mask. The nitride etched with the exposed portion of the top Si on each SOI wafer and etched in KOH solutions of varying temperature. To assure the samples free of particulate and other airborne contaminants, the experiment was conduced in a clean room environment.

The first step in this experiment is removal of masking contaminant simply by chemical methods by various chemicals. RCA scientific cleaning was adopted. An electronic grade chemical was taken. There are many process parameters that can be varied during the etching process. The composition employed in this study was a mixture of Hydrofluoric, Nitric, Sulfuric and Phosphoric acids in the ratios of 1:6:1:2 was chosen for an optimization process to this study. Silicon wafer thickness measurement was done on the MTI Proforma 300SA using MTI's exclusive Push/Pull™ capacitance technology. Automated scans across the complete wafer surface mapping of their thickness before and after etching for constant time was chosen in this study.

**Results and Discussion**

**Silicon Etching**

The chemistry most commonly used for isotropic wet etching of silicon is a combination of nitric acid and hydrofluoric acid. It is very often referred to as the HNA system (HF:Nitric:Acetic) with Acetic acid is added as a buffer for wet bench application. The nitric acid acts as an oxidizer to convert the surface into silicon dioxide and then the HF etches (dissolves) the oxide. The reaction proceeds as shown below and has been well documented in the literature [11].

$$Si + 4HNO_3 \rightarrow SiO_2 + 4NO_2 + 2H_2O$$
$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O$$

Although the above equations are quite simple, the actual etch rates of silicon are dependent upon the ratios of the chemicals in the mixture and also upon many processing parameters [12]. A

single wafer spin processor provides the capability to etch one side of the wafer while protecting the other side. Use in a single wafer spin processor, the addition of chemicals with higher viscosities is needed to provide more uniform etch over the wafer surface. The Acetic acid in the above solution is replaced by a combination of Phosphoric and Sulfuric acids. These thick viscous acids do not chemically participate in the etching reaction and therefore do not alter the chemical kinetics, but do increase the mass-transfer resistance as a result of the increase in the viscosity. It has been reported in the literature [13] that the addition of a few viscous acids to the mixture of HF and Nitric will decrease the roughness of the wafer more efficiently for the same removal rate. In addition, the ratios of the HF and Nitric can affect the etch rates and surface roughness. At high HF and low nitric concentrations the process is very temperature dependent and reaction rate controlled resulting in unstable silicon surfaces. At low HF and high nitric content, smooth polished surfaces result due to the more diffusion limited reaction. The rate of chemical reaction along with the spin process parameters have significant effect on the overall uniformity and surface finish that results from the process. Therefore, it is of utmost importance to keep the chemical mixture consistent from wafer to wafer and batch to batch in order to obtain repeatable silicon wafer etching results.

**Anisotropic Silicon Etching**

Strong alkaline substances (pH > 12) such as aqueous KOH-solutions to etch Si, so that

$Si + 4\ OH^- \rightarrow Si(OH)_4 + 4e^-$.

Since the bonding energy of Si atoms is different for each crystal plane, and KOH Si etching is not diffusion but etch rate limited, Si etching is highly anisotropic: While the (100) and (110) crystal planes are being etched, the stable (111) planes act as an etch stop: **(111)** orientated Si-wafers are almost not attacked by the etch. **(100)** orientated wafers form square-based pyramids with (111) surfaces. These pyramids are realised on Si solar cells for the purpose of reflection minimization. **(110)** orientated wafers form perpendicular trenches with [111] side-wall microchannels in micromechanics and microfluidics. The degree of anisotropy (etch rate selectivity between different crystal planes), the etch rates, and the etching homogeneity depend on the etching temperature, atomic defects in the silicon crystal, intrinsic impurities of the Si crystal, impurities (metal ions) by the etchant, and the concentration of Si atoms already etched. The doping concentration of the Si to be etched also strongly impacts on the etching: During etching, Boron doped Si forms borosilicate glass on the surface which acts as etch stop if the boron doping concentration exceeds 1019 $cm^{-3}$.

**Isotropic Etching of Silicon and $SiO_2$**

The following chemical reactions summarize the basic etch mechanism for isotropic silicon etching using $HF/HNO_3$ etching mixture:

(1) $NO_2$ formation: $HNO_2 + HNO_3 \rightarrow 2NO_2 + H_2O$

(2) Oxidation of silicon by $NO_2$: $2\ NO_2 + Si \rightarrow Si_2+ + 2NO_2$

(3) Formation of $SiO_2$: $SiO_2+ + 2(OH)^- \rightarrow SiO_2 + H_2$

(4) Etching of $SiO_2$: $SiO_2 + 6\ HF \rightarrow H_2SiF_6 + 2H_2O$

As we have seen, $HNO_3$ oxidizes Si, and HF etches the $SiO_2$ hereby formed. High HF: $HNO_3$ ratios promote rate-limited etching (strong temperature dependency of the etch rate) of Si via the oxidation 1-3, while low HF: $HNO_3$ ratios promote diffusion-limited etching (lower temperature dependency of the etch rate) via step (4). $HNO_3$ free HF etches do not attack Si. The $SiO_2$ etch rate is determined by the HF-concentration, since the oxidation 1- 3 does not account. Compared to thermal oxide, deposited (e. g. CVD) $SiO_2$ has a higher etch rate due to its porosity; wet oxide a slightly higher etch rate than dry oxide for the same reason. An accurate control of the etch rate requires a temperature control within ± 0.5°C. Dilution with acidic acid improves wetting of the hydrophobic Si surface and thus increases and homogenizes the etch rate. Doped (n- and p-type) silicon as well as phosphorus-doped $SiO_2$ etches faster than undoped Si or $SiO_2$.

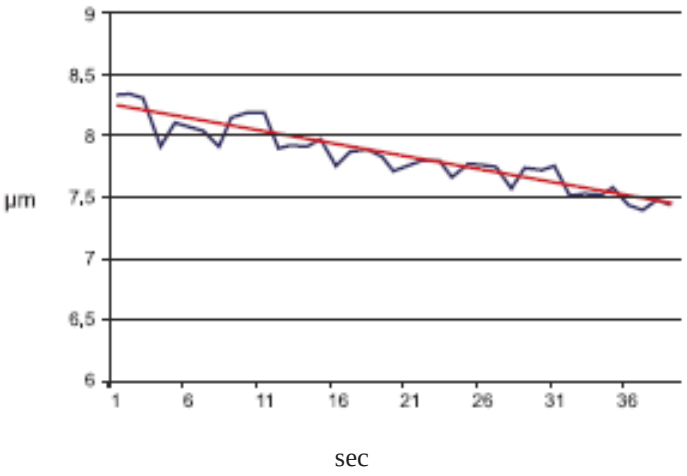


*Fig: silicon etch depth for constant etch time*

Over all, if we look at a physical interpretation for the silicon etching and decreasing etch rate we come up with the following equation as a possibility.

$$s = \frac{a}{bA}\{1 - e^{-bAt}\}$$

Where, S = silicon removed in µm,

a = initial etch rate,

b = constant parameter,

A = wafer area

Using this equation and comparing with the data we have obtained from the experiment are looking to be consistent. It should be noted that the above equation and resulting decrease in etch rate is dependent upon the wafer size (area of silicon being etched). For this investigation, wafer size was 150mm. For larger wafers the decrease in etch rate will be greater. To eliminate the variation in etch rate as wafers are processed we have two obvious options: increase the etching time or spike/replenish the active chemicals. Using the model and data we have acquired the following comparison. The data and model indicates that our etch rate is decreasing by 2.5% every 10 wafers. This translates into a 1 second increase in etch time after 4 wafers. The resulting etch rate is more consistent however the etch time and therefore tool throughput decreases. For a tool with an initial throughput of 25 wph, this would decrease to 15 wph after 16 hours (and 400 wafers) of processing.

While changeover from etch to rinse one should stop collecting the chemical in order to avoid the addition of water into the chemistry. The amount of chemical lost during this time (less than a second) is approximately 30ml at the flow rate we are using. Therefore, after processing 400 wafers we would have depleted the chemical supply by 12 liters and it would need to be refilled. Also at some point the amount of silicon in solution will be at a maximum and the chemistry will need to be replaced. Another way to maintain a constant etch rate is to either spike the chemical mixture with the active ingredient (HF) or to continuously remove and replenish the chemical solution or some combination of these. Our calculations are based on the 25 liter volume within our re-circulating chemical system. The ratio for filling the system with chemicals based on the chemical mix of 1:6:1:2 (Hydrofluoric, Nitric, Sulfuric and Phosphoric). Option one is to replace (remove and add) a percentage of the solution for every wafer. A second option is to spike with HF based on 10% of the initial solution volume and the 0.25% decrease in etch rate observed. However, this could not be done indefinitely due to some minimal loss of chemical during the switchover to water rinsing. The spiking with HF can be combined with adding enough of the chemical mixture to make up for the amount lost during changeover to the rinse cycle. Although both techniques will maintain a more stable etch rate, increasing the etch time will decrease the wafer throughput and require periodic shutdown for chemical disposal and refill resulting in lower system utilization. Chemical replenishment will maintain the wafer throughput; provide continuous chemical disposal and replenishment resulting in higher system utilization and overall lower cost of ownership.

**Conclusion**

There are many wet-chemical etch recipes known for etching silicon. These processes are used for a variety of applications including micromachining, cleaning, and defect delineation. The detailed behaviour and rate of the etchant will vary between laboratory environments and exact processes. As silicon wafers are etched a decrease in etch rate is observed. Spiking with HF provides a means to replenish the active component. At the same time, silicon is building up in the solution in the form of hexafluorosilicic acid. The wafer size is determine the spiking, removal and fresh make-up quantities for a stable equilibrium to be reached where the solution is self-replacing. This is the lowest

cost of ownership in terms of chemical costs and system down time and will result in a constant etch rate with time.

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